

# SSC8222GS1

## **N-Channel Enhancement Mode MOSFET**

#### $\geq$ Features

V <sub>DS</sub>	V <sub>GS</sub>	R <sub>DS(ON)</sub>	ID
20V	±12V	5.5mΩ@10V	45A
		7.5mΩ@4V5	437

#### Description $\geq$

This SSC8222GS1 uses advanced trench technology to provide excellent RDSON and low gate charge. The complementary MOSFETS may be used to form a level shifted high side switch, and for a host of other applications.

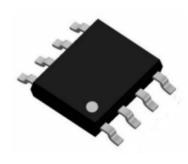
100% UIS + ΔVDS + Rg Tested!

- Applications  $\geq$
- DC/DC converters •
- Power supplies •
- Motor Drive Control •
- Synchronous rectification

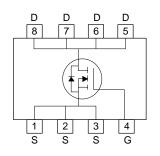
#### **Ordering Information** $\geq$

Device	Package	Shipping		
SSC8222GS1	SOP-8	2500/Reel		

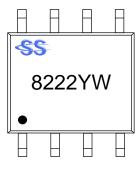
#### Pin configuration $\triangleright$



SOP-8



### Pin Configuration (Top View)



### Marking

(YW: Internal Traceability Code)





Symbol	Parameter		Ratings	Unit	
V <sub>DSS</sub>	Drain-to-Source Voltage		20	V	
V <sub>GSS</sub>	Gate-to-Source Voltage		±12	V	
	Continuous Drain Current <sup>d</sup>	Tc=25℃	45		
ID		Tc=100℃	25	A	
IDSM	Continuous Drain Current <sup>a</sup>	T <sub>A</sub> =25℃	15	A	
		T <sub>A</sub> =70℃	11		
Ідм	Pulsed Drain Current <sup>b</sup>		180	A	
_	Power Dissipation <sup>c</sup>	Tc=25℃	25	W	
PD		Tc=100℃	10		
Розм	Power Dissipation <sup>a</sup>	T <sub>A</sub> =25℃	2.5	W	
		T <sub>A</sub> =70℃	1.6		
Eas	Avalanche Energy <sup>b</sup> L=0.5mH Single Pulse		25	mJ	
TJ	Operation junction temperature		-55~150	°C	
Tstg	Storage temperature range		-55~150		

### > Absolute Maximum Ratings ( $T_A=25^{\circ}C$ unless otherwise noted)

### > Thermal Resistance Ratings ( $T_A=25^{\circ}C$ unless otherwise noted)

Symbol	Parameter	Ratings	Unit	
R <sub>0JA</sub>	Junction-to-Ambient Thermal Resistance <sup>a</sup>	50	°C/W	
R <sub>θJC</sub>	Junction-to-Case Thermal Resistance	5		

Note:

- a. The value of R<sub>θJA</sub> is measured with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz.copper, in a still air environment with T<sub>A</sub>=25 °C.The value in any given application depends on the user is specific board design. The power dissipation is based on the t≤10s thermal resistance rating.
- b. Repetitive rating, pulse width limited by junction temperature.
- c. The power dissipation P<sub>D</sub> is based on T<sub>J(MAX)</sub>=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.
- d. The maximum current rating is package limited.





# > Electrical Characteristics (T<sub>A</sub>=25 $^{\circ}$ C unless otherwise noted)

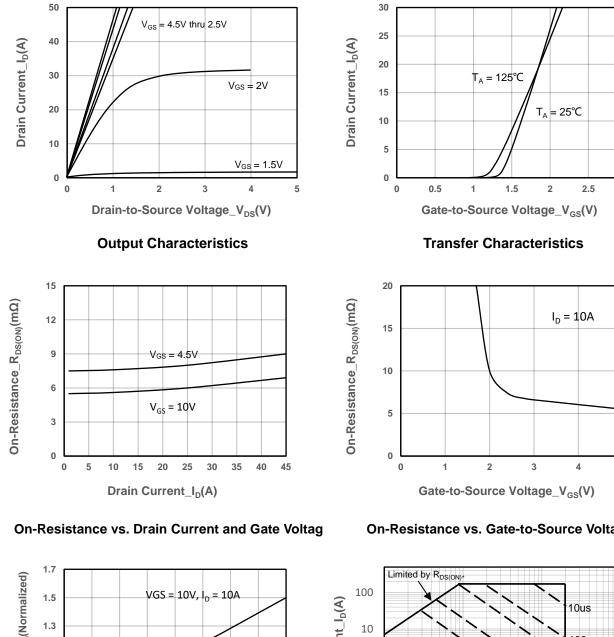
Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit
Drain-Source Breakdown Voltage	V <sub>(BR)</sub> dss	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250µA	20			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250 uA$	0.4	0.7	1.2	V
	RDS(on)	$V_{GS} = 4.5 V, I_D = 10 A$		5.5	7.4	mΩ
Drain-Source On-Resistance		V <sub>GS</sub> = 2.5V, I <sub>D</sub> = 6A		7.5	10	
Zero Gate Voltage Drain Current	loss	$V_{DS} = 16V, V_{GS} = 0V$			1	μA
Gate-Source Leak Current	lgss	$V_{GS} = \pm 12V$ , $V_{DS} = 0V$			±100	nA
Transconductance	G <sub>FS</sub>	$V_{DS} = 5V, I_D = 10A$		25		s
Forward Voltage	Vsd	$V_{GS} = 0V$ , $I_S = 1A$		0.8	1.3	V
Gate Resistance	Rg	$V_{DS} = 0V, f = 1MHz$		2		Ω
Input Capacitance	Ciss			1420		pF
Output Capacitance	Coss	V <sub>DS</sub> = 10V, V <sub>GS</sub> = 0V, f = 1MHz		240		
Reverse Transfer Capacitance	Crss			210		
Total Gate Charge	Q <sub>G</sub>			13		nC
Gate to Source Charge	Q <sub>GS</sub>	$V_{GS} = 4.5V, V_{DS} = 10V,$		5		
Gate to Drain Charge	$Q_{GD}$	I <sub>D</sub> = 10A		6		
Turn-on Delay Time	T <sub>D(ON)</sub>			11		
Rise Time	Tr	$V_{GS} = 4.5V, V_{DS} = 10V,$ $R_L = 1\Omega, R_G = 1\Omega$		22		- ns
Turn-off Delay Time	T <sub>D(OFF)</sub>			35		
Fall Time	T <sub>f</sub>			17		
Diode Recovery Time	Trr	I <sub>F</sub> =10A, di/dt=100A/us		11		ns
Diode Recovery Charge	Qrr	I <sub>F</sub> =10A, di/dt=100A/us		15		nC

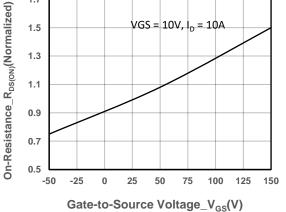


3

5

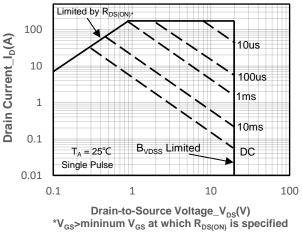
#### Typical Performance Characteristics ( $T_A=25^{\circ}C$ unless otherwise noted) $\triangleright$





**On-Resistance vs. Junction Temperature** 

**On-Resistance vs. Gate-to-Source Voltage** 



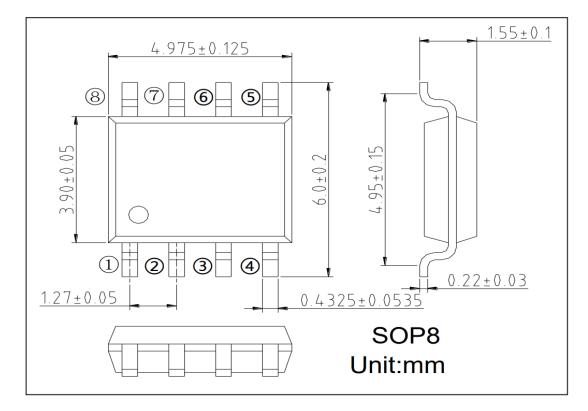
Safe Operating Area vs. Junction-to-Ambient

SSC-V1.0

/ 5 Δ



## Package Information



### DISCLAIMER

SSCSEMI RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. SSCSEMI DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICIENCE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

THE GRAPHS PROVIDED IN THIS DOCUMENT ARE STATISTICAL SUMMARIES BASED ON A LIMITED NUMBER OF SAMPLES AND ARE PROVIDED FOR INFORMATIONAL PURPOSE ONLY. THE PERFORMANCE CHARACTERISTICS LISTED IN THEM ARE NOT TESTED OR GUARANTEED. IN SOME GRAPHS, THE DATA PRESENTED MAY BE OUTSIDE THE SPECIFIED OPERATING RANGE (E.G. OUTSIDE SPECIFIED POWER SUPPLY RANGE) AND THEREFORE OUTSIDE THE WARRANTED RANGE.

OUR PRODUCT SPECIFICATIONS ARE ONLY VALID IF OBTAINED THROUGH THE COMPANY'S OFFICIAL WEBSITE, CRM SYSTEM, OR OUR SALES PERSONNEL CHANNELS. IF CHANGES OR SPECIAL VERSIONS ARE INVOLVED, THEY MUST BE STAMPED WITH A QUALITY SEAL AND MARKED WITH A SPECIAL VERSION NUMBER TO BE VALID.